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IP4035CX24

10-channel integrated filter network with ESD input protection to IEC 61000-4-2 level 4

Rev. 01 — 12 February 2010 Product data sheet

1. Product profile

1.1 General description

The IP4035CX24 is a 10-channel RC low-pass filter array which is designed to provide filtering of undesired RF signals. In addition, the IP4035CX24 incorporates diodes to provide protection to downstream components from ElectroStatic Discharge (ESD) voltages as high as ±30 kV contact according the IEC 61000-4-2 standard, far exceeding level 4.

The IP4035CX24 is fabricated using monolithic silicon technology and integrates 10 resistors and 20 diodes in a single Wafer-Level Chip-Scale Package (WLCSP). These features make the IP4035CX24 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

1.2 Features and benefits

- Pb-free, RoHS compliant and free of halogen and antimony (Dark Green compliant)
- 10-channel integrated π-type RC filter network
- 1 kΩ series resistance; 100 pF (typical) channel capacitance
- Integrated ESD protection withstanding ±30 kV contact discharge, far exceeding IEC 61000-4-2 level 4
- WLCSP with 0.5 mm pitch

1.3 Applications

Reduce ElectroMagnetic Interference (EMI) and Radio Frequency Interference (RFI) and provide downstream ESD protection for:

- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Other appliances with low frequency signals (e.g. keypads)

2. Pinning information

2.1 Pinning

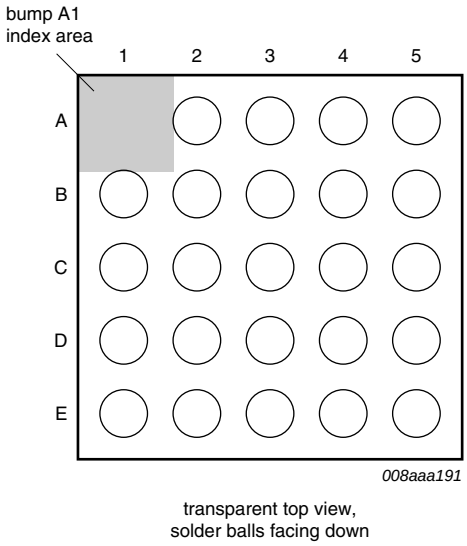


Fig 1. Pin configuration IP4035CX24

2.2 Pin description

Table 1. Pinning

Pin	Description
B1 and D1	filter channel 1
A2 and D2	filter channel 2
B2 and D3	filter channel 3
A5 and D4	filter channel 4
B5 and D5	filter channel 5
C1 and E1	filter channel 6
C2 and E2	filter channel 7
C3 and E3	filter channel 8
C4 and E4	filter channel 9
C5 and E5	filter channel 10
A3, A4, B3, B4	ground
A1	no ball

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3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4035CX24	WLCSP24	wafer level chip-size package; 24 bumps; 2.45 × 2.41 × 0.65 mm	IP4035CX24

4. Functional diagram

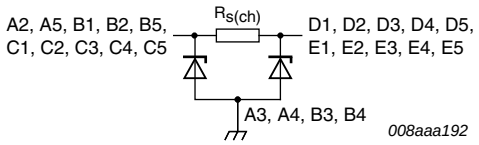


Fig 2. Schematic diagram IP4035CX24

5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			−0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	all pins to ground				
		contact discharge	[1]	−30	+30	kV
		air discharge	[1]	−30	+30	kV
		IEC 61000-4-2 level 4; all pins to ground				
		contact discharge		−8	+8	kV
		air discharge		−15	+15	kV
I_{ch}	channel current (DC)	current flow between external and internal pins		-	7	mA
P_{ch}	channel power dissipation	continuous power		-	42	mW
P_{tot}	total power dissipation	continuous power		-	420	mW
T_{stg}	storage temperature			−55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum		-	260	°C
T_{amb}	ambient temperature			−45	+85	°C

[1] Device is qualified with 1000 pulses of ±15 kV contact discharges each, according to the IEC 61000-4-2 model and far exceeds the specified level 4 (8 kV contact discharge).

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6. Characteristics

Table 4. Channel characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance		900	1000	1100	Ω
C_{ch}	channel capacitance	$V_{bias(DC)}$ = 0 V; f = 1 MHz	40	50	60	pF
V_{BR}	breakdown voltage	I_{test} = 1 mA	6	-	15	V
I_{LR}	reverse leakage current	per channel; V_I = 3.0 V	-	-	20	nA

Table 5. Frequency characteristics

T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
α_{il}	insertion loss	800 MHz < f < 3 GHz; R_{gen} = 50 Ω; R_L = 50 Ω	-	25	-	dB
α_{ct}	crosstalk attenuation	800 MHz < f < 3 GHz; R_{gen} = 50 Ω; R_L = 50 Ω	-	−25	-	dB

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7. Application information

7.1 Insertion loss

The insertion loss measurement configuration of a typical 50 Ω NetWork Analyzer (NWA) system for evaluation of the IP4035CX24 is shown in Figure 3.

The insertion loss of all channels for frequencies up to 6 GHz is displayed in Figure 4.

The insertion loss is measured with a test PCB utilizing laser drilled micro-via holes that connect the PCB ground plane to the IP4035CX24 ground pins.

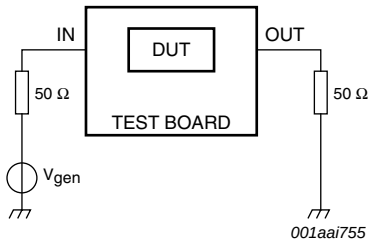
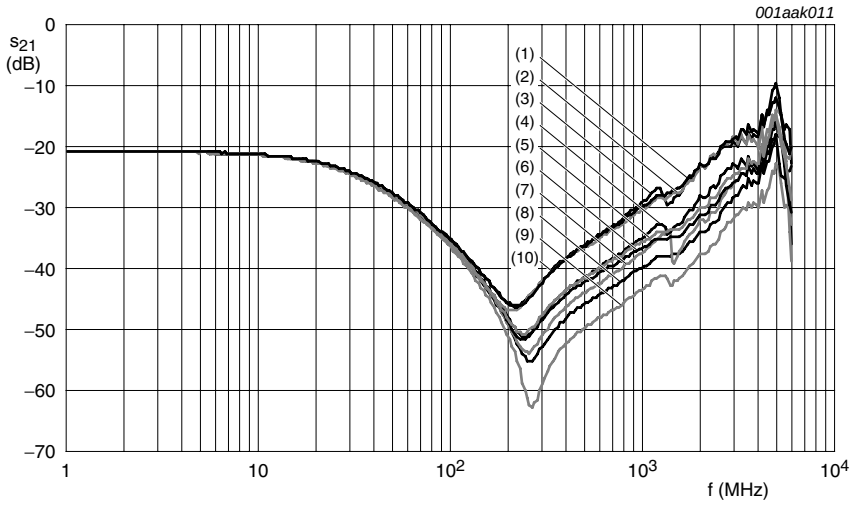


Fig 3. Frequency response measurement configuration



(1) Channel 1 (pins B1 and D1).
(2) Channel 10 (pins C5 and E5).
(3) Channel 6 (pins C1 and E1).
(4) Channel 5 (pins B5 and D5).
(5) Channel 9 (pins C4 and E4).
(6) Channel 8 (pins C3 and E3).
(7) Channel 3 (pins B2 and D3).
(8) Channel 2 (pins A2 and D2).
(9) Channel 4 (pins A5 and D4).
(10) Channel 7 (pins C2 and E2).

Fig 4. Measured insertion loss magnitudes

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7.2 Crosstalk

The crosstalk measurement configuration of a typical 50 Ω NWA system for evaluation of the IP4035CX24 is shown in Figure 5.

The measured crosstalk within the IP4035CX24 in a 50 Ω NWA system from one channel to another is shown in Figure 6 for two different pairs of channels representing both the worst and the best case conditions in terms of physical distance. In both cases the signal input pin is C1. While pin E2 is very close to the input, pin E5 is relatively far away. In all cases, unused connections are terminated with 50 Ω to ground.

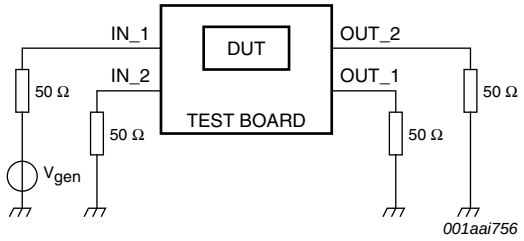
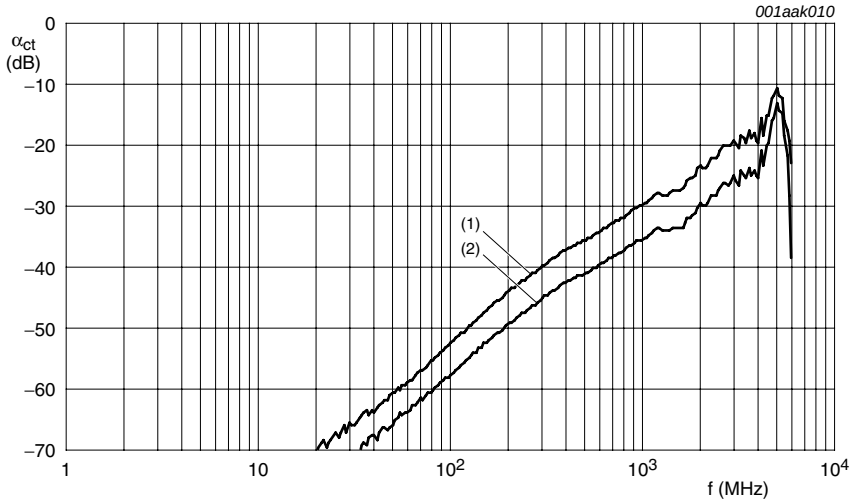


Fig 5. Crosstalk measurement configuration



(1) Channels 6 and 7 (pins C1 and E2).

(2) Channels 6 and 10 (pins C1 and E5).

Fig 6. Measured crosstalk between adjacent channels

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8. Package outline

WLCSP24: wafer level chip-size package; 24 bumps (5 x 5 - A1)

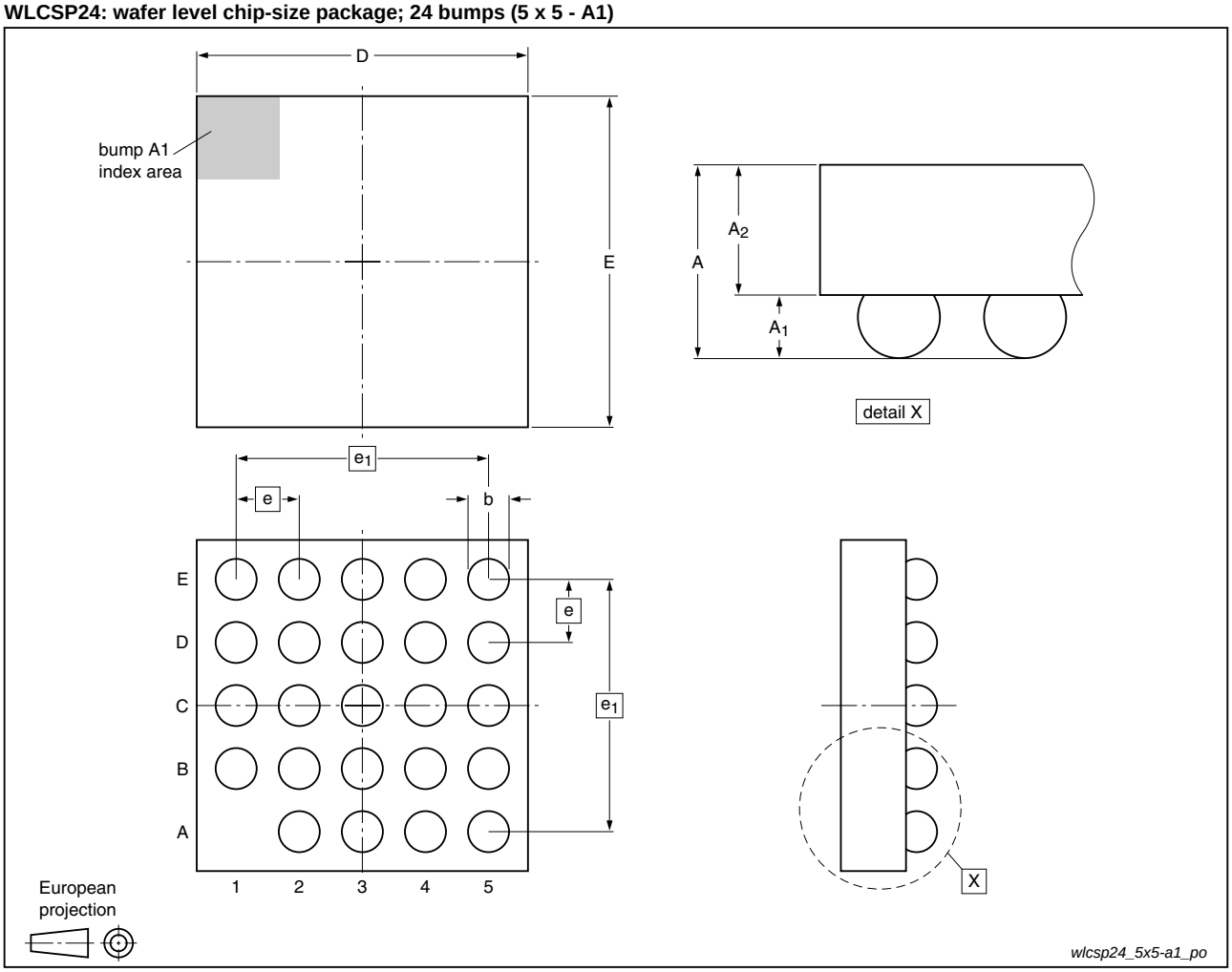


Fig 7. Package outline IP4035CX24 (WLCSP24)

Table 6. Dimensions for Figure 7

Symbol	Min	Typ	Max	Unit
A	0.60	0.65	0.70	mm
A_1	0.22	0.24	0.26	mm
A_2	0.38	0.41	0.44	mm
b	0.27	0.32	0.37	mm
D	2.40	2.45	2.50	mm
E	2.36	2.41	2.46	mm
e	-	0.5	-	mm
e_1	-	2.0	-	mm

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9. Design and assembly recommendations

9.1 PCB design guidelines

For optimum performance it is recommended to use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to Table 7 for the recommended PCB design parameters.

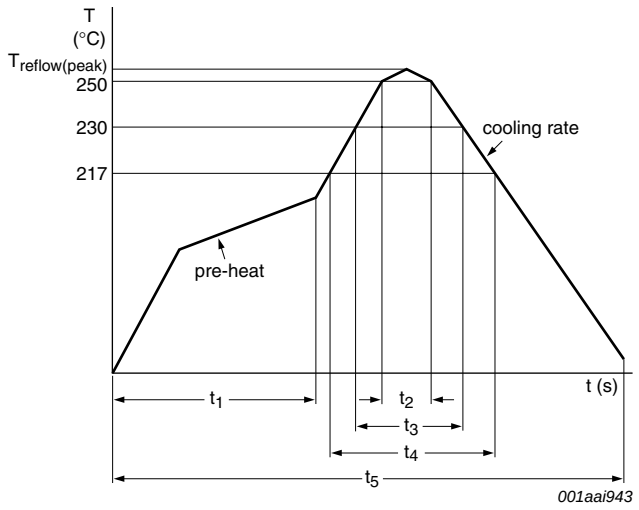
Table 7. Recommended PCB design parameters

Parameter	Value or specification
PCB pad diameter	200 μm
Micro-via diameter	100 μm (0.004 inch)
Solder mask aperture diameter	370 μm
Copper thickness	20 μm to 40 μm
Copper finish	AuNi
PCB material	FR4

9.2 PCB assembly guidelines for Pb-free soldering

Table 8. Assembly recommendations

Parameter	Value or specification
Solder screen aperture diameter	330 μm
Solder screen thickness	100 μm (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder / flux ratio	50 / 50
Solder reflow profile	see Figure 8



The device is capable of withstanding at least three reflows of this profile.

Fig 8. Pb-free solder reflow profile

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Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{reflow(peak)}$	peak reflow temperature		230	-	260	°C
t_1	time 1	soak time	60	-	180	s
t_2	time 2	time during T ≥ 250 °C	-	-	30	s
t_3	time 3	time during T ≥ 230 °C	10	-	50	s
t_4	time 4	time during T > 217 °C	30	-	150	s
t_5	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	–6	°C/s
		pre-heat	2.5	-	4.0	°C/s

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
NSMD	Non-Solder Mask PCB Design
PCB	Printed-Circuit Board
PCS	Personal Communication System
RFI	Radio Frequency Interference
RoHS	Restriction of Hazardous Substances
WLCSP	Wafer-Level Chip-Scale Package

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4035CX24_1	20100212	Product data sheet	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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